CLAIMS

What is claimed is:

1. A method of fabricating a polymer memory device in a via comprising:

providing a semiconductor substrate having at least one metal-containing layer thereon;

forming at least one dielectric layer over the metal-containing layer;

forming at least one via in the dielectric layer to expose at least a portion of the metal containing layer;

forming a polymer material in a lower portion of the via; and

forming a top electrode material layer in an upper portion of the via.

2. The method of claim 1, wherein the metal-containing layer is formed by a damascene process.

3. The method of claim1, wherein the dielectric layer comprises at least one of oxide, nitride, TEOS, FTEOS, and organic materials.

4. The method claim 1, further comprising forming at least one copper contact in the metal containing layer, the copper contact being any one of copper connection, copper pad, copper plug, and copper bit line.

5. The method of claim 1, wherein forming a polymer material in a lower portion of the via comprises converting at least a portion of the exposed metal containing layer to a metal sulfide and at least one of selective polymer growth by CVD, spin-on polymer solution and bake, and polymer growth by application of a monomers solution.

6. The method of claim 1, wherein the polymer material comprises polyphenol acetylene, poly-acetylene, poly-diphenyl acetylene, polyaniline,

polythiophene, polyporphyrins, porphyrinic macrocycles, thiol derivatized polyporphyrins, poly-metallocenes, polyferrocenes, polyphthalocyanines, polyvinylenes, polypyrroles, and poly-(p-phenylene vinylene, and/or combinations thereof, and/or monomers thereof.

7. The method of claim 1, wherein the top electrode material is a conductive material.

8. The method of claim 1, wherein the top electrode materials comprises tungsten (W), titanium (Ti), tantalum (Ta), titanium nitride (TiN), amorphous carbon, aluminum, indium-tin oxide, platinum, zinc, nickel, iron, manganese, magnesium, gold, chromium, metal silicides, alloys thereof, and/or any combination thereof.

9. The method of claim 8, wherein alloys comprise Hastelloy®, Kovar®, Invar, Monel®, Inconel®, brass, stainless steel, magnesium-silver alloy, and/or combinations thereof.

10. The method of claim 1, further comprising polishing the top electrode layer so as to form a top electrode plug in the upper portion of the via.

11. The method of claim 1, further comprising forming a word line over at least the top electrode.

12. The method of claim 1, further comprising forming a barrier metal layer immediately over at least the top electrode.

13. The method of claim 1, further comprising forming at least one of plugs, shallow trench isolation regions, and channel stop regions below the polymer material in the via.

14. A method of fabricating a polymer memory device in a via comprising:

providing a semiconductor substrate having at least a first dielectric layer thereon;

forming at least one of a copper bit line and a copper pad in the first dielectric layer;

forming at least a second dielectric layer over the at least one of the copper bit line and the copper pad;

forming at least one via in the second dielectric layer to expose at least a portion of the at least one copper bit line and copper pad;

growing a polymer material in a lower portion of the via;

forming a top electrode material layer in an upper portion of the via; and

forming a word line over at least the top electrode layer.

15. The method of claim 14, wherein the dielectric layer comprises at least one of oxide, nitride, TEOS, FTEOS, and organic materials.

16. The method of claim 14, wherein forming a polymer material in a lower portion of the via comprises converting at least a portion of the exposed copper to copper sulfide and at least one of selective polymer growth by CVD, spin-on polymer solution and bake, and polymer growth by application of a monomers solution.

17. The method of claim 14, wherein the polymer material comprises polyphenol acetylene, poly-acetylene, poly-diphenyl acetylene, polyaniline, polythiophene, polyporphyrins, porphyrinic macrocycles, thiol derivatized polyporphyrins, poly-metallocenes, polyferrocenes, polyphthalocyanines, polyvinylenes, polypyrroles, and poly-(p-phenylene vinylene, and/or combinations thereof, and/or monomers thereof.

18. The method of claim 14, wherein the top electrode materials comprises tungsten (W), titanium (Ti), tantalum (Ta), titanium nitride (TiN), amorphous carbon, aluminum, indium-tin oxide, platinum, zinc, nickel, iron, manganese, magnesium, gold, chromium, metal silicides, alloys thereof, and/or any combination thereof. The method of claim 1, further comprising polishing the top electrode layer so as to form a top electrode plug in the upper portion of the via.

19. The method of claim 14, further comprising polishing the top electrode layer so as to form a top electrode plug in the upper portion of the via.

20. A system of fabricating a polymer memory device in a via comprising: method of fabricating a polymer memory device in a via comprising:

means for providing a semiconductor substrate having at least a first dielectric layer thereon;

means for forming at least one of a copper bit line and a copper pad in the first dielectric layer;

means for forming at least a second dielectric layer over the at least one of the copper bit line and the copper pad;

means for forming at least one via in the second dielectric layer to expose at least a portion of the at least one copper bit line and copper pad;

means for growing a polymer material in a lower portion of the via;

means for forming a top electrode material layer in an upper portion of the via; and

means for forming a word line over at least the top electrode layer.